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PATENT
Attorney Docket No.: SYNOP-00701

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Bruce Harmon et al.

Serial No.: 09/637,984

Filed: August 11, 2000

For: **METHOD AND APPARATUS FOR
MODELING USING A
HARDWARE-SOFTWARE CO-
VERIFICATION ENVIRONMENT**

) Group Art Unit: 2763

) Examiner:

) **TRANSMITTAL LETTER**

) 162 N. Wolfe Road
) Sunnyvale, CA 94086
) (408) 530-9700

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APR 22 2002

Technology Center 2100

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed please find a Supplemental Information Disclosure Statement, Form PTO-1449, copies of the references contained thereon for filing in the U.S. Patent and Trademark Office.

The Commissioner is hereby authorized to charge any additional fee or credit overpayment to our Deposit Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 4-11-02

By: Thomas B. Haverstock

Thomas B. Haverstock
Reg. No.: 32,571

Attorneys for Applicants

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

- 1 -

HAVERSTOCK & OWENS LLP.

Date: 4-12-02 By: John D. Rasmussen



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**SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT**

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Sunnyvale, CA 94086
(408) 530-9700

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The citations listed below, copies attached, may be material to the examination of the above-identified application, and are therefore submitted in compliance with the duty of disclosure defined in 37 C.F.R. §§ 1.56 and 1.97. The Examiner is requested to make these citations of official record in this application.

The following printed publication is referred to in the body of the specification:

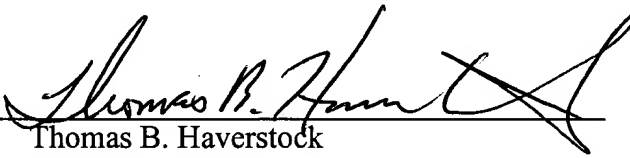
- Logic Modeling Corporation, LM Division, "Simulation Integration Manual" Aug. 1992, pp. i-xiii, and pp. 1-208..
- Logic Modeling Corporation, LM Division, "LM- Family User's Manual: Hardware Modeler Manual," Sept. 1993, pp. i-xviii and pp. 1-1 to Index
- Synopsys, Inc. "LM-1400 Systems, Hardware Modeling Manual," http address: "www.synopsys.com/products/lm/hw_models/lm_1400.htm," Oct. 13, 1997, pp. 1-4.
- Synopsys, Inc., "LM-Family Modeler Manual," March 2000, pp. 1-183.
- Synopsys, Inc., "Hardware Models, ModelSource 3000 Series and Options," http address "www.synopsys.com/products/lm/hw_models/hw_systems.htr," Oct. 13, 1997, pp. 1-9.

- Applied Microsystems Corp., Co-Verification Presentation Slides, 1998, pp.1-17.
- Carner, Larry & Eaglei HW/SW Co-Verification., "Viewlogic Software Group, Providing Solutions for Embedded Systems," 1997, pp. 1-7.
- Bunza, J. Geoffrey, Viewlogic Systems, Inc., "The Magic of Building HW/SW Systems," 1997, pp. 1-143.

This Supplemental Information Disclosure Statement under 37 C.F.R. §§ 1.56 and 1.97 is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that anyone or more of these citations constitutes prior art.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 4/11/02

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Thomas B. Haverstock
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